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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/856,212	05/18/2001	Kozo Nakamura	82821	6761

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Welsh & Katz  
22nd Floor  
120 South Riverside Plaza  
Chicago, IL 60606-3913

[REDACTED] EXAMINER

SONG, MATTHEW J

[REDACTED] ART UNIT

[REDACTED] PAPER NUMBER

1765

DATE MAILED: 11/05/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

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<b>Office Action Summary</b>	Application No.	Applicant(s)
	09/856,212	NAKAMURA ET AL.
	Examiner Matthew J Song	Art Unit 1765

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1) Responsive to communication(s) filed on \_\_\_\_\_.

2a) This action is **FINAL**.                    2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4) Claim(s) 1-5, 7 and 9-13 is/are pending in the application.

4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.

5) Claim(s) \_\_\_\_\_ is/are allowed.

6) Claim(s) 1-5, 7 and 9-13 is/are rejected.

7) Claim(s) \_\_\_\_\_ is/are objected to.

8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) The proposed drawing correction filed on \_\_\_\_\_ is: a) approved b) disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some \* c) None of:

1. Certified copies of the priority documents have been received.

2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.

3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) The translation of the foreign language provisional application has been received.

15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) <input type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____	6) <input type="checkbox"/> Other: _____

**DETAILED ACTION*****Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claim 1 and 4-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iida et al (US 5,968,264).

Claims 4 and 5 have been added to the header, this is not a new grounds of rejection because the examiner clearly intended to include the claims in the previous rejection by referring to claims 4 and 5 in the previous rejection.

Iida et al teaches a single crystal ingot of silicon was pulled while varying the average pulling rate over a range of 1.0 mm/min and 0.4 mm/min. Iida et al also teaches the temperature gradient in an in-crystal descending temperature zone between a melting point of silicon and 1400°C in the vicinity of the solid-liquid interface was set as follows:  $G_e=45.0\text{ }^{\circ}\text{C}/\text{cm}$  and  $G_c=42.0\text{ }^{\circ}\text{C}/\text{cm}$ , where  $G_e$  reads on applicant's G outer and  $G_c$  reads on applicant's G center. The ratio of  $G_e/G_c$  can be determined to 1.07 and at a pulling rate of 0.72 mm/min the V/G at the center is  $0.16\text{ mm}^2/\text{ }^{\circ}\text{C} \cdot \text{min}$  and at the outer periphery is  $0.17\text{ mm}^2/\text{ }^{\circ}\text{C} \cdot \text{min}$  (col 14, ln 20-67).

Iida does not teach temperature gradient in a pulling axis direction within a temperature range from silicon melting point to 1350°C. It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Iida by attempting to optimize the temperature range by conducting routine experimentation.

Referring to claim 4, Iida et al is silent to a silicon wafer with decreased grown-in defects, which is obtained from the silicon ingot of claim 1. It is inherent to Iida's invention to produce a silicon wafer with decreased grown-in defects because Iida teaches similar growth conditions of a silicon single crystal ingot as applicant.

Referring to claim 5, Iida et al is silent to a silicon perfect single crystal wafer free from grown-in defects obtained from the silicon ingot of claim 1. It is inherent to Iida's invention to produce a silicon wafer with decreased grown-in defects because Iida teaches similar growth conditions of a silicon single crystal ingot as applicant.

3. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Iida et al (US 5,968,264) in view of Luter et al. (US 5,922,127).

Iida et al teaches all of the limitations of claim 2, except the conditions (a) and (b) of claim 1 are adjusted by changing a distance between a heat shielding element equipped in a Czochralski method-based silicon single crystal production device and silicon melt.

In an apparatus for pulling single crystals, Luter et al teaches a crucible mounted on a motorized turntable which raises the crucible to maintain the surface of the molten source material at a constant level as the ingot grows and the source material is removed from the melt (col 3, ln 60-65). Luter et al also teaches a heat shield (40) mounted above the upper surface of the molten source material (col 4, ln 32-37). Luter et al discloses the a heat shield may be positioned within the crucible above the melt for conserving heat at the interface between the ingot and molten material to prevent heat loss from the melt surface, which reduces the instantaneous axial thermal gradient  $G_o$  (col 2, ln 15-25), therefore Luter reads on applicant's

limitation of adjusting conditions by changing the distance between a heat shielding element and the silicon melt. It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Iida et al with Luter to avoid undesired changes in the thermal profile during the growth process.

4. Claims 1 and 3-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hourai et al (US 5,954,873).

Claims 3-5 have been added to the header, this is not a new grounds of rejection because the examiner clearly intended to include the claims in the previous rejection by referring to claims 3-5 in the previous rejection.

Hourai et al teaches the relationship of V/G and the position in the radial direction of the crystal in Fig 2, where V is the single crystal pulling rate (mm/min) and the inside-crystal temperature gradient in the direction of the pulling axis in a high temperature zone from the melting point of silicon to 1300°C. Hourai et al also teaches the single crystal pulling rate and the inside-crystal temperature gradient in the axial direction are two critical parameters for controlling the diameter of an oxidation-induced stacking fault (OSF) ring and the diameter of the OSF ring can be determined by the ratio of V/G (col 4, ln 50-60). Hourai discloses to compensate for changes in the temperature gradient of the crystal, the pulling rate is adjusted so that a constant V/G may be achieved (col 6, ln 55-60).

Hourai does not teach the parameter of a  $V/G=0.16-0.18 \text{ mm}^2/\text{°C}\cdot\text{min}$  or a  $G_{\text{outer}}/G_{\text{center}} \leq 1.10$ . It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Hourai by deriving the condition of claim 1, based on the profile of Fig 2.

Hourai does not teach temperature gradient in a pulling axis direction within a temperature range from silicon melting point to 1350°C. It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Hourai by attempting to optimize the temperature range by conducting routine experimentation.

Referring claim 3, Hourai discloses to compensate for changes in the temperature gradient of the crystal, the pulling rate is adjusted so that a constant V/G may be achieved (col 6, ln 55-60).

Referring to claim 4, Hourai et al is silent to a silicon wafer with decreased grown-in defects, which is obtained from the silicon ingot of claim 1. It is inherent to Iida's invention to produce a silicon wafer with decreased grown-in defects because Iida teaches similar growth conditions of a silicon single crystal ingot as applicant.

Referring to claim 5, Hourai et al is silent to a silicon perfect single crystal wafer free from grown-in defects obtained from the silicon ingot of claim 1. It is inherent to Iida's invention to produce a silicon wafer with decreased grown-in defects because Iida teaches similar growth conditions of a silicon single crystal ingot as applicant.

5. Claim 7 is rejected under 35 U.S.C 103(a) as being unpatentable over Kim et al (US 5,942,032) in view of Luter (5,922,127).

Kim et al teaches a heat shield assembly for use in a crystal puller of the type used to grow monocrystalline silicon ingots according to the Czochralski method. Kim et al also teaches a crystal puller (12) includes a shell for isolating an interior, which includes a lower crystal growth chamber, this reads on applicant's limitation of a closed container. Kim et al discloses a

quartz crucible containing a molten semiconductor source, where the crucible is mounted on a turntable for rotation about a vertical axis and is capable of being raised with the growth chamber. Kim et al also discloses heating panels (24) heat the crucible (col 4, 42-67). Kim et al also teaches the heat shield assembly an intermediate heat shield (40), a lower heat shield (42) and an upper heat shield (36) (col 5, ln 15-65) and the heat shield assembly can be raised and lowered using the existing pulling mechanism of the crystal puller (12) (col 3, ln 15-20). Kim et al discloses the upper heat shield is positioned so that the portions of the ingot entering the upper heat shield are approximately at 1150°C and inside the upper heat shield, heat transfer from the ingot to the sidewalls is reduced so that the instantaneous axial temperature gradient  $G_o$  is lessened in the portion of the upper heat shield (col 9, ln 40-50 and ln 25-27). Kim et al also discloses the lower heat shield prevents heat from radiating from the sidewalls of the crucible to the ingot (col 9, ln 15-22). Kim et al also discloses using the heat assembly (10) a high  $v/G_o$  ratio is achieved and the ratio of  $v/G_o$  is increased without changing the pull rate  $v$ , however variation in the pull rate may be employed to increase the  $v/G_o$  ratio (col 9, ln 55-67 and col 10, ln 1-10)

Kim et al does not teach a pulling element for pulling a silicon single crystal ingot, while rotating

In a method of pulling a monocrystalline ingot used to manufacture semiconductor wafers, Luter et al discloses a pulling mechanism (30) rotates a seed crystal C and moves it up and down through the growth chamber (col 4, ln 5-10). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Kim with Luter because counter-rotating the crystal and crucible prevents the exchange of impurities between the melt directly below the crystal and the residual melt, note Chapter 2.5 of Zulehuler and Huber

The combination of Luter and Kim does not teach the intended use of the device is for adjusting a ratio V/G of a pulling speed V in the Czochralski method to an average value G of the in-crystal temperature gradient in a pulling axis direction within a temperature range from the silicon melting point to 1350°C to within a range of 0.16 to 0.18 mm<sup>2</sup>/°C min and a ratio G outer/g center is 1.10 or less, but a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. The combination of Luter and Kim teaches all of the structure features of the device, as applicant, therefore is capable of performing the intended use.

6. Claims 9-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adachi et al. (US 5,931,662).

Claims 12 and 13 have been added to the header, this is not a new grounds of rejection because the examiner clearly intended to include the claims in the previous rejection by referring to claims 12 and 13 in the previous rejection.

Adachi et al teaches the preferred annealing conditions for forming defect-free region, where defect-free reads on applicant's perfect crystal, is to ramp up to a temperature in excess of 1100°C and annealing preformed at temperatures ranging from 500°C to 900°C for more than 10 minutes can provide IG functions by forming oxide precipitates, BMD. Adachi et al also teaches BMD for IG functions can also be formed by ramping up from 500°C to 900°C at a rate of 0.5°C/min (col 10, ln 60-67) Adachi et al discloses maintaining a temperature between 500°C to

900°C for more than 10 minutes during the ramp down process following sustained heating at a temperature in excess of 1100°C makes it possible to provide IG functions by forming BMD at a rate of 0.5°C/min (col 11, ln 5-15). Adachi et al also discloses silicon single crystal wafers were loaded into an annealing boat and into a furnace pre-heated to 700°C (col 11, ln 50-60). Adachi teaches in Fig 11 and 12 indicating the relationship between surface depth and oxygen concentration and the results indicate DZ layers had been secured in all wafers after annealing (col 12, ln 46-55).

Adachi et al does not teach a heat treatment temperature at the initial entry of the silicon single crystal wafer to be a target of the heat treatment is 500°C or less. It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Adachi by attempting to optimize same by conducting routine experimentation.

Referring to claim 10, Adachi is silent to a uniform distribution of an oxide precipitate density of the silicon single crystal wafer after heat treatment. It is inherent to Adachi's invention to uniform the distribution of an oxide precipitate density of the silicon single crystal wafer after heat treatment because Adachi teaches a similar heat treatment with an ultimate temperature set in a range of 500-900°C at a similar ramping rate of 0.5 °C/min as applicant.

Referring to claim 11, Adachi is silent to adjusting the distribution of an oxide precipitate density of the silicon single crystal wafer after the heat treatment. It is inherent to Adachi's invention to uniform the distribution of an oxide precipitate density of the silicon single crystal wafer after heat treatment because Adachi teaches a similar heat treatment with an ultimate temperature set in a range of 700-900°C as applicant.

Referring to claim 12, Adachi teaches the oxygen concentration is less than  $13 \times 10^{17}$  atoms/cm<sup>3</sup> in the DZ layer in Figs 11 and 12. If Adachi does not teach this in Figs 11 and 12, then it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Adachi by attempting to optimize same by conducting routine experimentation.

Referring to claim 13, Adachi teaches silicon wafers were annealed under similar conditions as taught by applicant.

***Response to Arguments***

7. Applicant's arguments filed 9/9/2002 have been fully considered but they are not persuasive.

The arguments regarding the Iida et al reference concerning claims 1 and 4-5 are not deemed persuasive. It is not fully understood why one of ordinary skill in the art would perform the complicated mathematical calculations in applicant's argument. When one of ordinary skill in the art can determine the ratio of G outer/ G inner can be determined to be 1.07 and the ratio V/G ratio at a center portion to a crystal out periphery position to be 0.16 and 0.17 mm<sup>2</sup>/°C\*min, respectively for pulling velocity and temperature gradients disclosed by Iida et al. Iida et al discloses a G outer of 45.0 °C/cm and a G inner of 42.0 °C/cm and a pulling rate of 0.72 mm/min and the ratio can merely be determined by division

The arguments regarding the Hourai et al reference concerning claims 1 and 3-5 are not deemed persuasive. Applicant's argument that Hourai et al does not contemplate the temperature, where the examiner interprets temperature to refer to the temperature gradient, of the crystal at the outer surface of the crystal is inaccurate, Hourai et al teaches controlling a V/G ratio in at the

center of a crystal and at an outer surface of a crystal, where G is a temperature gradient (col 3, ln 40-67), therefore Hourai et al is concerned with the temperature at the outer surface of the crystal. Regarding Figure 2, Hourai et al teaches figure 2 is a graph showing the relationship of V/G between the position in a radial direction of a crystal and the V/G level with the slope of the V/G curve effecting the development of defects (col 3, ln 15-25). Figure 2 refers to V/G at the center and at an outer surface, where V is constant; therefore the ratio of the temperature can merely be determined by the ratio of V/G at the center and at the outer surface from Figure 2.

The arguments regarding the Adachi et al reference are not deemed persuasive. Adachi et al teaches growing a crystal, slicing wafers, etching the wafer in aqueous solutions and annealing the wafers after etching in Embodiment 1. Adachi et al does not explicitly teach an initial wafer temperature range of 500°C or less, as admitted previously, but the etching operation in an aqueous solution clearly takes place at a temperature less than 500°C and therefore the wafer clearly enters at a temperature less than 500°C. It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Adachi et al by optimizing temperature to obtain a range of 500°C or less by conducting routine experimentation.

### ***Conclusion***

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a)

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

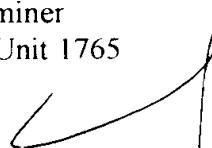
9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew J Song whose telephone number is 703-305-4953. The examiner can normally be reached on M-F 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Benjamin L Utech can be reached on 703-308-3868. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9310 for regular communications and 703-872-9311 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0661.

Matthew J Song  
Examiner  
Art Unit 1765

MJS  
November 1, 2002

  
ROBERT KUNEMUND  
PRIMA  
PFR